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09/828,573	04/02/2001	Ramesh Duvvuru	388682000700	6602

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EXAMINER	
CASIANO, ANGEL L	
ART UNIT	**PAPER NUMBER**
2182	6

DATE MAILED: 02/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/828,573	Applicant(s) DUVVURU, RAMESH	
	Examiner Angel L. Casiano	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 13-15* is/are rejected.

7)☒ Claim(s) *10-12 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The present Office action is in response to application filed 02 April 2001.

2. Claims 1-18 are pending in the application.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

- "first column 210", "SPE 200", "POH data 210" (see page 2, lines 11-13; Figure 1).
- "pipeline 402", "pipeline 404"(see page 11, lines 11, 19, 26, 28-29; Figure 4)

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description:

- Figure 1, "110", "112".

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. Figure 1 should be designated by a legend such as --Prior Art—(see Page 3, line 26) because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing

correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said first plurality of bytes processed by a *neighboring byte processing engine* is designated as a delineation byte". However, the claim does not mention a neighboring engine. Claims 2-6 depend from claim 1 and are therefore rejected under the same basis.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-3, 7-9 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hadziomerovic [EP 0147086] in view of Bagheri et al., "10 Gb/s Framer/Demultiplexer IC for SONET STS-192 Applications", 1995 IEEE.

Regarding claim 1, Hadziomerovic teaches an apparatus for processing bytes received from a data stream (see Abstract). The cited art teaches receiving data (bytes) from a data channel during clock cycles (see page 2, lines 22-35). Hadziomerovic also teaches an apparatus capable of generating data regarding the status of the bytes (see page 8, line 11; page 23, lines 3-29). Hadziomerovic clearly teaches the indication of a flag byte (see Abstract; Figure 1, "10", "20"). The cited art discloses using flags for designating delineating bytes (see page 1, line 21; Figure 1; page 2, lines 1-5). Nonetheless, Hadziomerovic teaches serial, instead of parallel processing, as claimed. In addition, the cited art does not explicitly teach an "input formatter" as disclosed in the claims. Regarding these limitations, Bagheri teaches a data stream, where serial data is converted into "a byte-parallel, frame-synchronized output data stream" (see Abstract). One of ordinary skill in the would have been motivated to apply parallel communication, as disclosed by Bagheri et al., since the disclosure teaches bandwidth optimization (see Introduction) in a SONET (Synchronous Optical Network) environment.

As for claim 2, Hadziomerovic teaches a status register (see page 8, lines 11-20). In addition, the prior art teaches using flags for designating delineating bytes (see page 1, line 21; Figure 1; page 2, lines 1-5).

As for claim 3, Hadziomerovic discloses status registers (see page 8, lines 11-12). The cited art also uses flags for designating delineating bytes (see page 1, line 21; Figure 1; page 2, lines 1-5). The cited disclosure includes delineation for the frames (see HDLC, Figure 1).

Regarding claim 7, Hadziomerovic exposes an apparatus for processing bytes received from a data stream (see Abstract). The cited art teaches receiving data (bytes) from a data channel during a cycle (see page 2, lines 22-35). Hadziomerovic also teaches an apparatus capable of generating byte status data (see page 8, line 11; page 23, lines 3-29). Hadziomerovic clearly teaches the indication of a flag byte (see Abstract; Figure 1, "10", "20"). The cited art discloses using flags for designating delineating bytes (see page 1, line 21; Figure 1; page 2, lines 1-5). Nonetheless, Hadziomerovic teaches serial, instead of parallel processing (as claimed). In addition, the cited art does not explicitly teach "input formatter means" as recited in the claim. Regarding these limitations, Bagheri teaches a data stream, where serial data is converted into "a byte-parallel, frame-synchronized output data stream" (see Abstract). One of ordinary skill in the would have been motivated to apply parallel communication, as disclosed by Bagheri et al., since the disclosure teaches bandwidth optimization (see Introduction) in a SONET (Synchronous Optical Network) environment.

As per claim 8, Hadziomerovic teaches status register means (see page 8, lines 11-20). In addition, the prior art teaches using flags for designating delineating bytes (see page 1, line 21; Figure 1; page 2, lines 1-5).

As for claim 9, Hadziomerovic exposes status register means (see page 8, lines 11-12). The cited art also uses flags for designating delineating bytes (see page 1, line 21; Figure 1; page 2, lines 1-5). The cited disclosure includes delineation for the frames (see HDLC, Figure 1).

Regarding claims 13-15, these constitute the method of processing bytes received from a data stream. The claimed method includes the steps of "receiving", "generating", and "processing". The combination of prior art cited in the present Office action teaches or suggests the limitations corresponding to the apparatus (see Rejections above) and therefore, the method. Accordingly, these claims are rejected under the same rationale.

Allowable Subject Matter

10. Claims 4-6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. Accordingly, these claims are objected to in the present Office action.

11. Claims 10-12 and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In consideration of claims 4-5, 10-11 and 16-17, the prior art does not teach or suggest, alone or in combination a "write *enable status bit* for respective ones of said plurality of bytes identified as *valid data*". In addition, the prior art does not include an *input formatter* for generating a *byte*

status code for each of a first plurality of bytes identified as *valid data.* Furthermore, the references do not disclose an "*input register FIFO* coupled to the input formatter".

As for claims 6, 12 and 18, the apparatuses disclosed in the prior art do not include "*a plurality of quad-byte processors*" for calculating *"cell delineation values"*.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- *A SONET STS-3c User Network Interface Integrated Circuit*, [Robe, Thomas J. Vol. 9, No. 5, June 1991, IEEE.] Teaches a CMOS chip which functions as an STS-3c transmitter and receiver and can interface to the STS-3c line in either bit-serial or byte-parallel data format.
- Begur et al. [US 5,784,649] teaches a transfer controller which maintains status information relating to the status of data in the memory blocks.
- Bernardini [US 5,144,623] discloses a system for receiving and processing HDLC frames.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 703-305-8301. The examiner can normally be reached on 9:30-6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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12 February 2004.